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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,717	12/28/2001	Timothe Litt	1662-52800 JMH (P01-3848)	1520

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EXAMINER	
BONURA, TIMOTHY M	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,717	LITT, TIMOTHE	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,6,7,12-16,21,25 and 27* is/are allowed.

6)☒ Claim(s) *5,8-11,17-20,22-24,26,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6-7, 12-16, 21, 25, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Davis, U.S. Patent Number 6,618,775.

3. Regarding claim 1:

a. Regarding the limitation of "an on-chip logic analyzer," Davis discloses a system with a bus watch circuit that monitors data. (Lines 44-46 of Column 2).

b. Regarding the limitation of "a cache memory that includes a plurality of cache sets," Davis discloses a system with multiple circular buffers. (Lines 47-49 of Column 4).

c. Regarding the limitation of "at least one on-chip logic device that stores data to said plurality of cache sets during normal operation," Davis discloses a system that can stored data to memory during operation of the processor. (Lines 48-51 of Column 2).

d. Regarding the limitation of "a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and which disables at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer," Davis discloses a system

with circular buffers that store data until a trigger event occurs. (Lines 50-52 of Column 4).

4. Regarding claim 2, Davis discloses a system with a processor with on-chip logic device included within the processor. (Lines 42-44 of Column 3).

5. Regarding claim 3, Davis discloses a system with trigger signals that are produced by event match circuitry. The event match circuitry is connected to the processors. (25-26 and 35-39 of Column 4).

6. Regarding claim 4, Davis discloses multiplexer which is enabled via the comparator that has input from the triggers sets. (Lines 59-67 of Column 5 and Lines 1-7 of Column 6).

7. Regarding claim 6, Davis discloses multiplexer which is enabled via the comparator that has input from the triggers sets. (Lines 59-67 of Column 5 and Lines 1-7 of Column 6).

8. Regarding claim 7, Davis discloses a set of 4 on-chip analyzers that can respond to the selection of the triggers from the event match data. (Figure 6, items 632,634,636,638).

9. Regarding claim 12:

e. Regarding the limitation of "a CPU core," Davis discloses a system with a processor with on-chip logic device included within the processor. (Lines 42-44 of Column 3).

f. Regarding the limitation of "a cache memory coupled to said CPU core, said cache memory including a plurality of cache sets that during normal operation stores data written to the CPU," Davis discloses a system with multiple circular buffers that stored data to memory during operation of the processor. (Lines 47-51 of Column 2).

g. Regarding the limitation of "a logic analyzer that receives information relating to the internal state of the processor, said logic analyzer coupled to at least one of said plurality of cache sets, and wherein said logic analyzer is capable of gaining ownership of said at least on each cache set to store selected portions of said received information when said logic analyzer is enabled," Davis discloses a system with circular buffers that store data until a trigger event occurs. (Lines 50-52 of Column 4).

10. Regarding claim 13, Davis discloses a system with trigger signals that are produced by event match circuitry. The event match circuitry is connected to the processors. (25-26 and 35-39 of Column 4). Davis discloses multiplexer which is enabled via the comparator that has input from the triggers sets. (Lines 59-67 of Column 5 and Lines 1-7 of Column 6).

11. Regarding claim 14, Davis discloses a system with trigger signals that are produced by event match circuitry. The event match circuitry is connected to the processors. (25-26 and 35-39 of Column 4).

12. Regarding claim 15, Davis discloses a system with a bus watch circuit that monitors data. (Lines 44-46 of Column 2).

13. Regarding claim 16, Davis discloses a system with trigger signals that are produced by event match circuitry. The event match circuitry is connected to the processors. (25-26 and 35-39 of Column 4). Davis discloses multiplexer which is enabled via the comparator that has input from the triggers sets. (Lines 59-67 of Column 5 and Lines 1-7 of Column 6).

14. Regarding claim 21:

h. Regarding the limitation of "a cache memory divided into a plurality of cache sets," Davis discloses a system with multiple circular buffers that stored data to memory during operation of the processor. (Lines 47-51 of Column 2).

i. Regarding the limitation of "test logic coupled to said cache memory, which tests the cache sets during system initialization and determines which cache sets are operative," Davis discloses a system with circular buffers that can send status signals to a TAP to note that data is ready to be uploaded. (Lines 41-52 of Column 10).

j. Regarding the limitation of "a cache controller that controls the storage and retrieval of data from said cache memory, with said cache controller only storing data to cache sets that are determined to be operative by the test logic," Davis discloses a system with circular buffers that can send status signals to a TAP to note that data is ready to be uploaded. (Lines 41-52 of Column 10).

k. Regarding the limitation of "a CPU core coupled to said cache memory, said CPU core storing data to all operative cache sets during normal operation," Davis discloses a system with multiple circular buffers that stored data to memory during operation of the processor. (Lines 47-51 of Column 2).

l. Regarding the limitation of "an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled," Davis discloses a system with circular buffers that store data until a trigger event occurs. (Lines 50-52 of Column 4).

15. Regarding claim 25:

m. Regarding the limitation of "enabling an on-chip logic analyzer to receive and select data for storage," Davis discloses a system with circular buffers that store data until a trigger event occurs. (Lines 50-52 of Column 4).

n. Regarding the limitation of "disabling a cache set from use by any device other than the on-chip analyzer," Davis discloses a system with trigger signals that are produced by event match circuitry. The event match circuitry is connected to the processors. (25-26 and 35-39 of Column 4). Davis discloses multiplexer which is enabled via the comparator that has input from the triggers sets. (Lines 59-67 of Column 5 and Lines 1-7 of Column 6).

o. Regarding the limitation of "storing said selected data in the disabled cache set," Davis discloses during testing data can be loaded into a cache that has enabled a trigger event. (Lines 55-63 of Column 10).

16. Regarding claim 27, Davis discloses a multiplexer that selects multiple event match circuits that supply data to the buffers. (Lines 35-40 of Column 4).

Allowable Subject Matter

17. Claims 5, 8-11, 17-20, 22-24, 26, and 28-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00.**
- The examiner can be reached at: **571-272-3654.**

19. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Rob Beausoliel.**

- The supervisor can be reached on **571-272-3645.**

20. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

22. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

23. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

NADEEM IQBAL
PRIMARY EXAMINER